A Silicon MOS Process for Integrated RF Power Amplifiers

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ABSTRACT

A silicon-based technology is presented which integrates passive components with a silicon Power MOSFET for use in Integrated Power Amplifiers at UHF, VHF, and RF frequencies. This low-cost process incorporates capacitors, inductors, resistors, ground vias, transmission lines, and an ESD protection diode. A design library containing models and layouts for the active and passive components was compiled.

INTRODUCTION

The integration of silicon microwave active devices with passive components has many advantages, most important of which are size reduction, lower cost, and improved circuit manufacturability. The trade-off typically associated with this integration is a degradation in the ideality of the passive components. The process described here was developed with the goal of minimizing this degradation while keeping the cost low. Series and shunt capacitors, inductors, resistors, and ESD diodes have been successfully integrated with an RF silicon MOSFET and used to design and fabricate Integrated Power Amplifiers (IPA's). This represents the first time that this has been done using a silicon-based MOS technology--not only is this cost effective but eliminates the need for the negative power supply required when using MESFET's. The applications of these IPA's include driver and output stages of the transmitters in pagers and cellular telephones at VHF, UHF, and RF frequencies. S-parameters and model parameters have been extracted for the MOS devices, capacitors, inductors, resistors, transmission lines, ESD structures, ground vias, and the input/output (I/O) pads.

PROCESS INTEGRATION

The fabrication of the silicon MOSFET follows conventional processing techniques. Self-aligned implants and a polysilicon gate are utilized. The gate is silicided so that a lower gate access resistance can be achieved. (This allows for higher power gain from the device.) The source of the FET is electrically connected to the backside of the chip, a highly doped p-type substrate which acts as the circuit's ground plane, through the ground via. The ground via consists of a high dose/energy p-type implant which is thermally driven until it merges with the p+ substrate (see Figure 1). This is a very inexpensive method for constructing a ground via. The discrete RF performance of this silicon MOS device has been previously reported. [1,2]

Due to the RF applications of the IPA, a thick oxide layer is used as the field isolation. This is important for the series capacitors and inductors which need to be fabricated as far away from the ground plane as possible to achieve reasonable Q-factors. The series capacitor is created by using the silicided polysilicon as the bottom plate and the first layer of metal (metal-1) as the top plate (see Figure 2). Nitride is used as the dielectric. The silicide reduces the parasitic resistance associated with the bottom plate of the capacitor. This coupled with the fact that the entire capacitor sits on the field oxide helps maximize the Q-factor. Also note that all of the layers used to make the series capacitor save the nitride dielectric are already used in the fabrication of the device. This keeps the process simple and cost-effective. The same holds for the shunt capacitor which uses the p+ ground via implant to act as its bottom plate as well as a shunt connection to ground (metal-1 is used as the top plate and nitride is used as the dielectric).

The inductors are fabricated using metal-2 stacked on top of metal-1 (see Figure 3). By stacking the metal a total inductor thickness of over 3μm is achieved. This reduces the parasitic resistance of the inductor and thus enhances

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the Q-factor without using expensive gold metallization. The entire inductor is fabricated on top of dielectric layers (ILD0) which are deposited on the field oxide. This results in a distance from metal-1 to the ground plane of over 6μm. Transmission line Q-factors are enhanced by using the same method (i.e. stacked metal layers are patterned over ILD0 and field oxide).

The resistors and ESD structures are integrated without the addition of any processing steps. By simply patterning the silicided polysilicon over the field oxide, the resistors are created. The ESD structures consist of a diode to ground formed by the n+ source/drain implant and the medium dose p-type channel implant. Connection to the ground plane is made by surrounding the structure with the ground via.

MODELING AND CHARACTERIZATION

All of the models for the active and passive components are supplied to designers as a design library for use in HP-MDS.

The silicon MOSFET's are simulated with a Root Model which is extracted from on-wafer S-parameters at 1GHz. Measured vs. model graphs for DC and S-parameter data are attached (Figure 4). The Root Model also accurately predicts the measured RF Output versus Input Power as well as Second and Third Order Harmonics.

The inductors are designed in spiral patterns. The values achieved range from 16nH to 1nH depending on the number of turns and the metal linewidth. Library models for these inductors were based on measured S-parameters (0.2-10.2Ghz) The Q-factors of these inductors are typically lower than 10 at 1GHz, depending on the specific design. Despite the non-ideal lossy nature of the silicon substrate, these inductors are suitable for input and interstage matching in IPA's. A similar modeling technique is used for the transmission lines. The performance of a 9-turn spiral inductor is illustrated in Figure 5.

A two-port lumped model is used for the series and shunt capacitors as well as the silicide polysilicon resistor and I/O pads. The lumped models are valid from DC up to 5 GHz. The ESD structure achieves a Human Body Model protection of about 450V and is designed to be directly attached to an I/O pad.

IPA RESULTS

In this section we present the measured and simulated RF characteristics of a 2-Stage 31.5 dBm IPA for 850MHz applications. A separate symposium submission includes a discussion on several aspects of the amplifier design: cell size choice, gate and drain biasing networks, ESD protection schemes and load line design. [3]

Figure 6 depicts the layout of the 850MHz 1.5W IPA and Figure 7 illustrates the measured Gain and Efficiency vs. Output Power for this design. The design achieved 31.5dBm output power with a gain of 19.5dB and power added efficiency (PAE) of 56.5%. The IPA was designed using the models for the active and passive components discussed in the previous sections and simulated in HP-MDS.

REFERENCES

[1] "Silicon MOSFETs, The Microwave Device Technology for the 90's", 1993 IEEE MTT-S International Microwave Symposium Digest, N. Camilleri, J. Costa, D. Lovelace, D. Ngo

[2] "New Development Trends for Silicon RF Device Technologies", IEEE 1994 Microwave and Millimeter Wave, N. Camilleri, J. Costa, D. Lovelace, D. Ngo

[3] "RF Silicon MOS Integrated Power Amplifiers for Analog Cellular Applications", submitted to 1996 IEEE MTT-S International Microwave Symposium, D. Ngo, W. Burger, J. Costa, C. Dragon, T. Gillenwater, E. Spears, M. Shields, D. Spooner, N. Camilleri

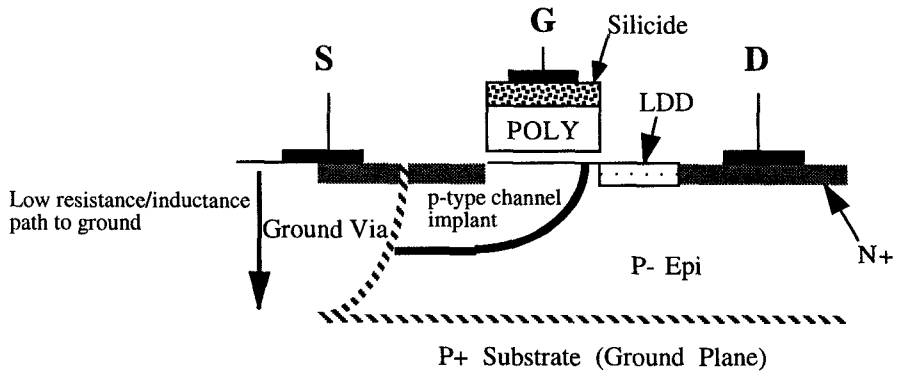

Figure 1: Silicon MOSFET Cross-Section

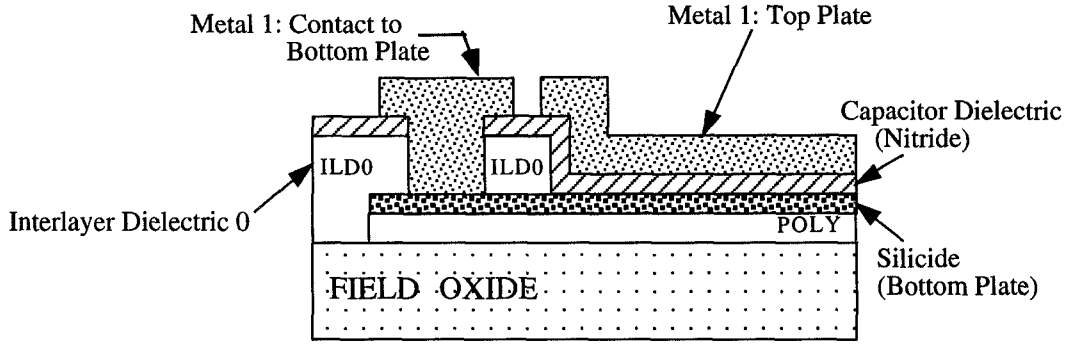

Figure 2: Series Capacitor Cross-Section

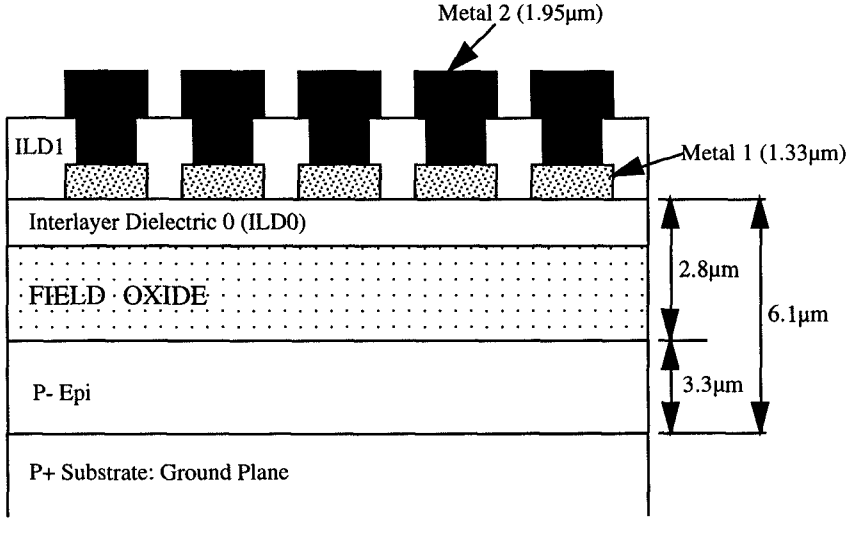

Figure 3: Inductor Cross-Section & Top View

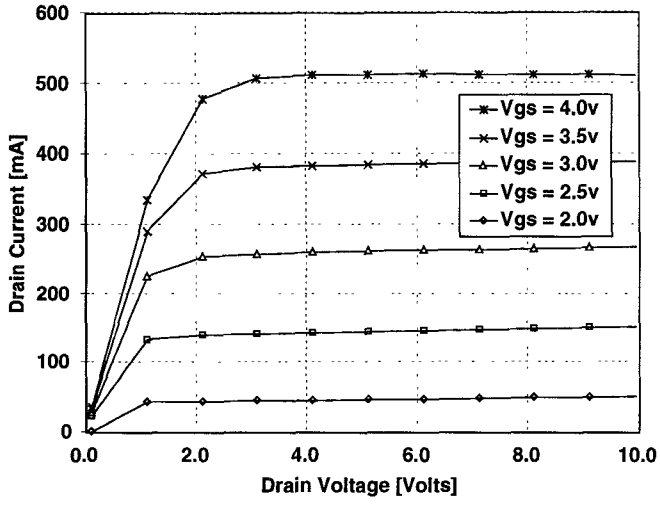

Figure 4a: MOSFET DC ID-vs-VDS Data

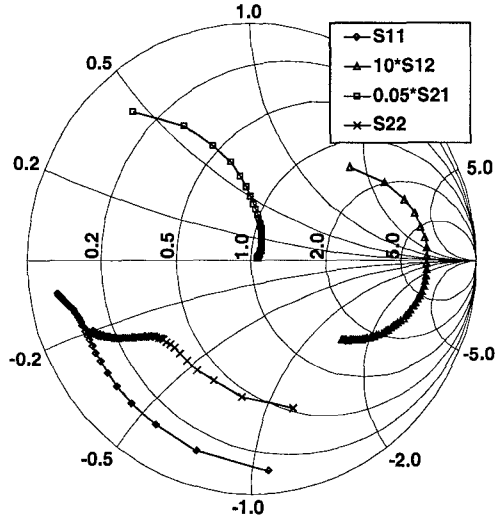

Figure 4a: MOSFET S-Parameter Data (VD=6V,VG=3*VT)

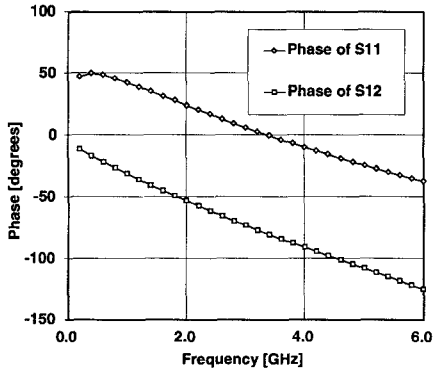

Figure 5: Spiral Inductor S-Parameters (9 turn layout)

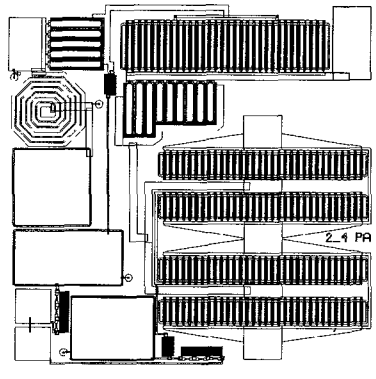

Figure 6: Layout of 850MHz 1.5W IPA

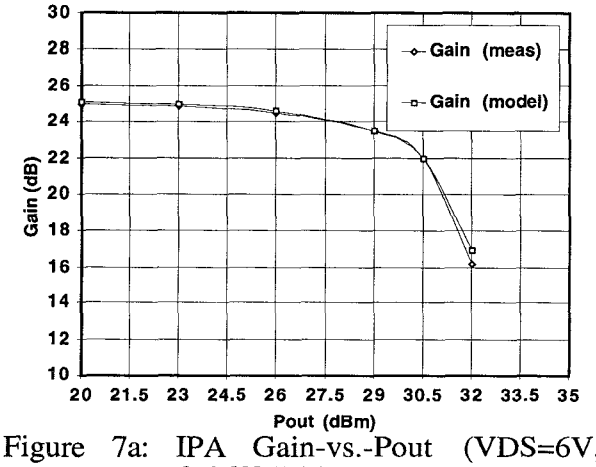

Figure 7a: IPA Gain-vs.-Pout (VDS=6V, f=850MHz)

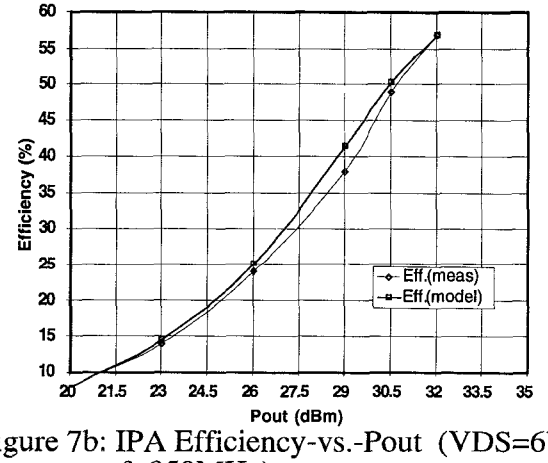

Figure 7b: IPA Efficiency-vs.-Pout (VDS=6V, f=850MHz)